BAE SYSTEMS

Reconfigurable, High Density, High Speed, Low Power, Radiation Hardened FPGA Technology MAPLD2008

S.Ramaswamy[1], Leonard Rockett[1],, Dinu Patel[1], Steven Danziger[1]
Rajit Manohar[2], Clinton W. Kelly, IV[2], John Lofton Holt[2], V. Ekanayake[2], Dan Elftmann[2]
Ken LaBel, Melanie Berg etc. NASA[3]
[1]BAE SYSTEMS, 9300 Wellington Road, Manassas, VA, 20110, USA
[2]Achronix Semiconductor Corporation, 333 W. San Carlos Street, San Jose, CA, 95110, USA
[3]NASA Goddard

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Agenda

- RHFPGA Roadmap
- RHFPGA Product Features
- Achronix Technology Overview
- BAE Radiation Hardened Process Technology Overview
- Program Status / Summary

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Radiation Hardened FPGA Roadmap

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Rad Hard FPGA Product

Past

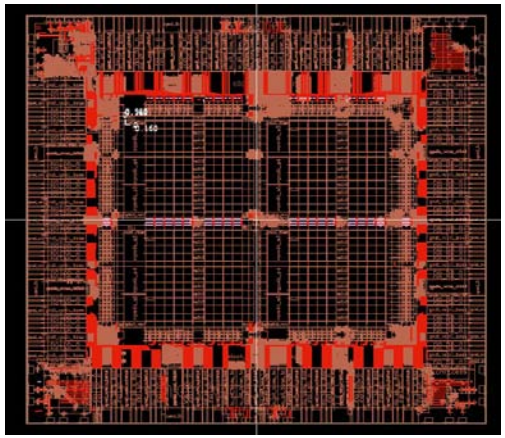
- **Heritage: Actel ONO RH1280 and RH1020**
  - **Anti-fuse technology, non-volatile**
  - **0.8µm RH CMOS, 5V Supply**
  - **In production since 1996, over 25,000 shipped**

Re-install in progress

Present

- **M2M Anti-fuse Technology:**
  - **250K-gate (RHAX250-S)**
  - **RH15 CMOS, 1.5V Core / 3.3V I/O**
  - **Flight Orders in 2009**

Entry Vehicle



Future

- **≥3M-gate, re-configurable, non-volatile**
- **Radiation Hardened, high speed**
- **RH15 CMOS, 1.5V Core / 3.3V I/O**
- **Projected qualification starts in 2009**

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RHFPGA Product Features

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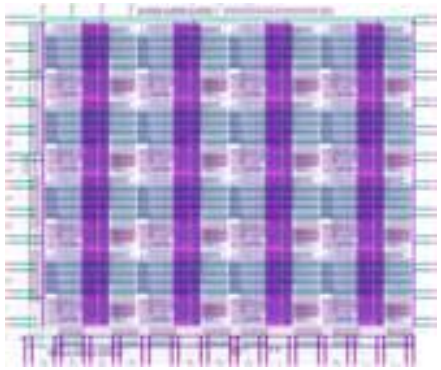
- TID tolerance of > 1Mrad Si
- SEU immunity < 10^{-11}errors/bit-day
- System speeds > 300MHz
- Support of RADHARD IOs and RAMs for integration into Systems
- Reconfigurable/Reprogrammable
- Low Power
- Extreme Temperature Operation
- Non Volatile
- EMP Protected
- Full Compatibility with Existing EDA Tools
- Product Name -> Radrunner



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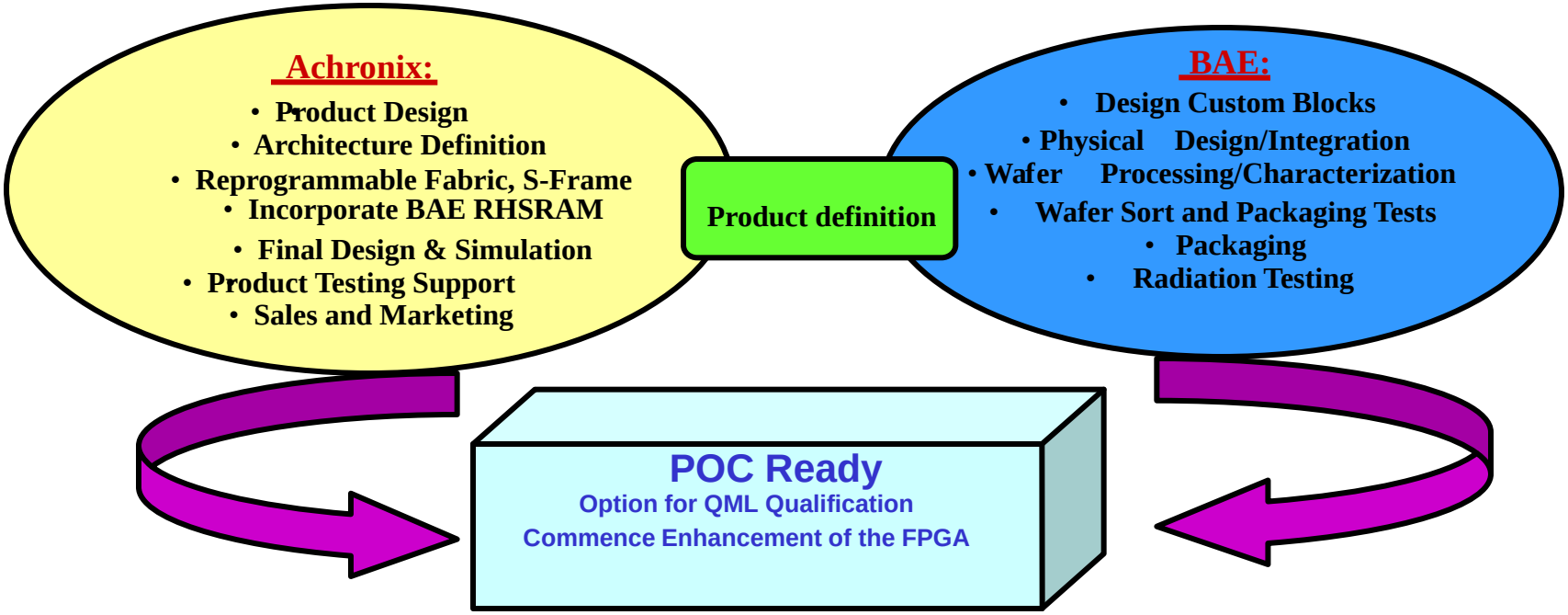
Achronix Company Overview

- Privately held fabless semiconductor company founded in New York in 2004
- Achronix has received $34.4M Series A funding
- Founders developed technology in 1998 at Cornell University
- Headquartered in San Jose, CA
- Working 90 and 180 nm prototype silicon
- Partnerships with the world leading foundry TSMC, BAE Systems and numerous IP & EDA vendors
- 65 nm commercial FPGA silicon has been received from TSMC; currently shipping
- All Key IP's protected by patents

Reconfigurable RHFPGA Proof of Concept

Key Roles to support Reconfigurable RHFPGA Proof of Concept:

ACX RHFPGA Product Development…. A collaborative effort



Achronix RHFPGA Technology

Achronix Core Technology

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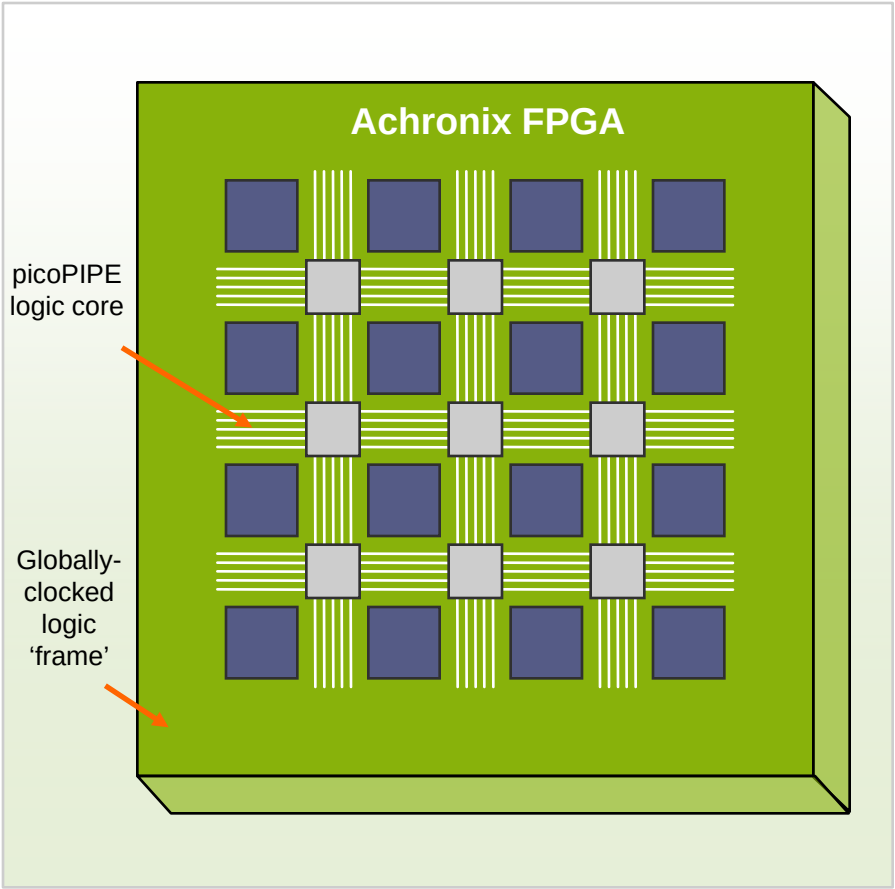
- Core contains ‘picoPIPE’ technology used for both logic and routing
  - You do not need to know the details in order to benefit from this
- Fully synchronous I/O ‘frame’ surrounds the core
- picoPIPE technology is used to implement synchronous hardware
  - A design is input using a HDL such as RTL
  - The RTL does not need to be targeted to picoPIPE technology



Looks like a regular FPGA, but has approx 4x throughput

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Data Tokens

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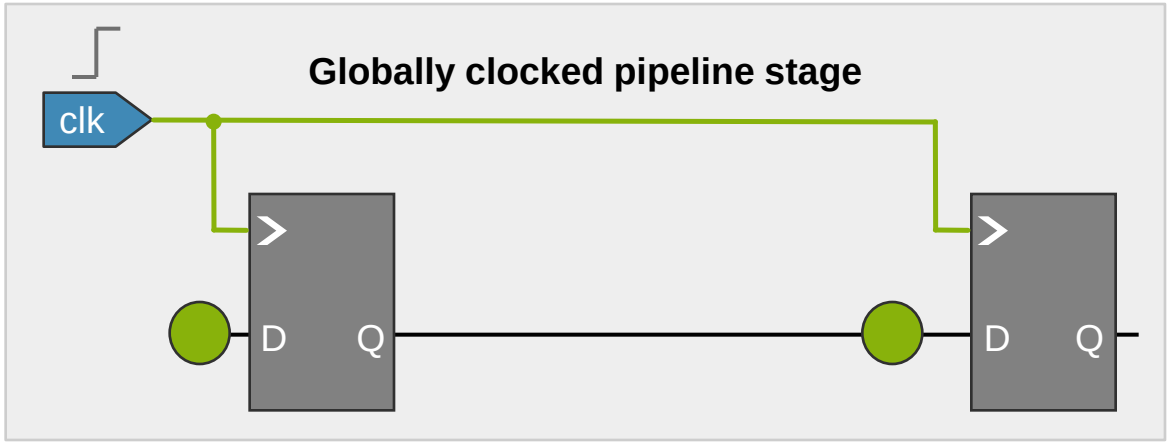
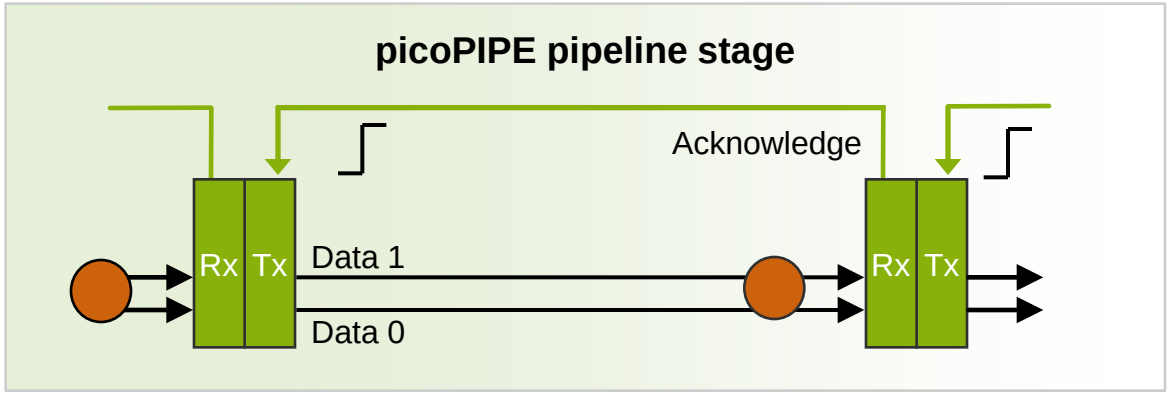
Traditional FPGA

- In globally-clocked logic, a data value at a clock edge can be considered as a "Data Token"
  - Only valid data (data at a clock edge) is propagated
  - Hence each register output's a new Data Token (value) at every clock edge



Achronix FPGA

- picoPIPE logic also contains Data Tokens
  - Each data token uses 2 signals instead of 1
  - Data validation (clock-like functionality) is performed using acknowledge instead of a global clock



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More on Throughput

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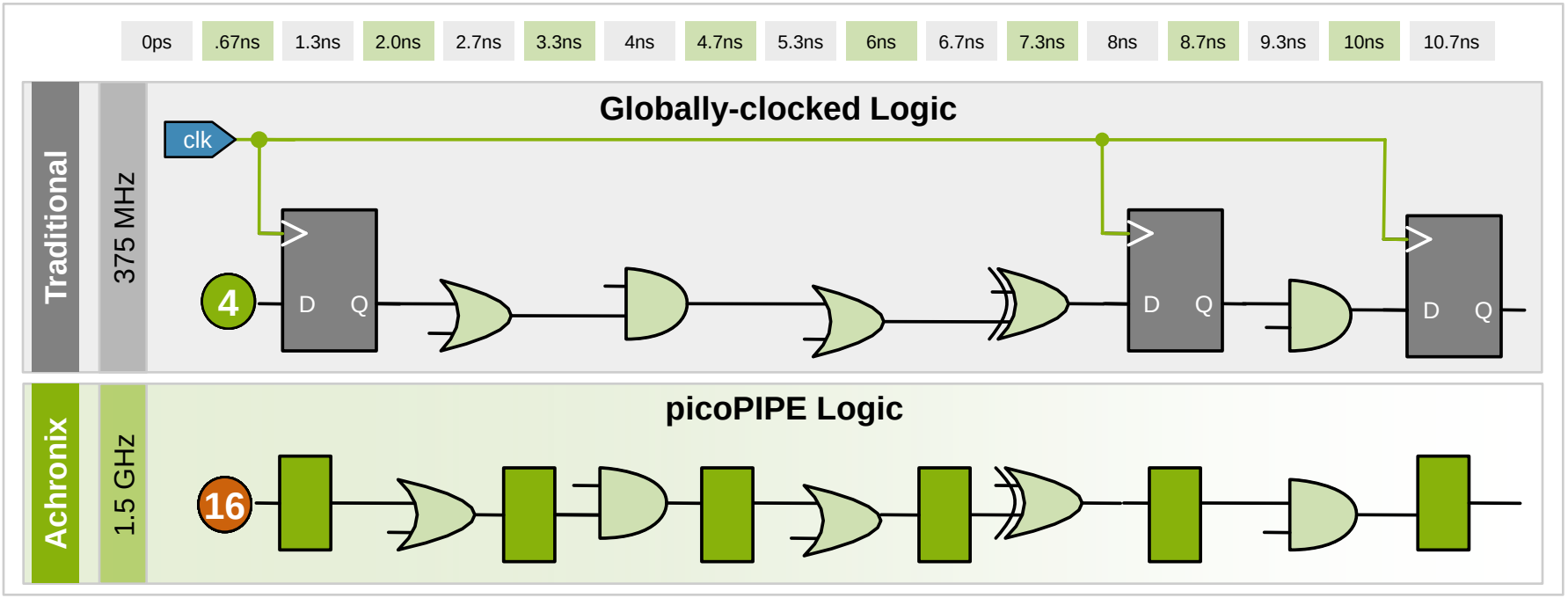
Traditional FPGA

- Globally Clocked Logic is not balanced
- The clock rate must allow for the slowest path in the entire clock domain
- Any combinatorial logic faster than the slowest path (by definition, all remaining logic) waits for the slowest one to finish

Achronix FPGA

- Achronix technology allows fine-grained pipelining
- Allows data rate to be much faster
- Pipelining also allows more data values in flight
- Equates to faster throughput



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Familiar Silicon & Familiar Tools

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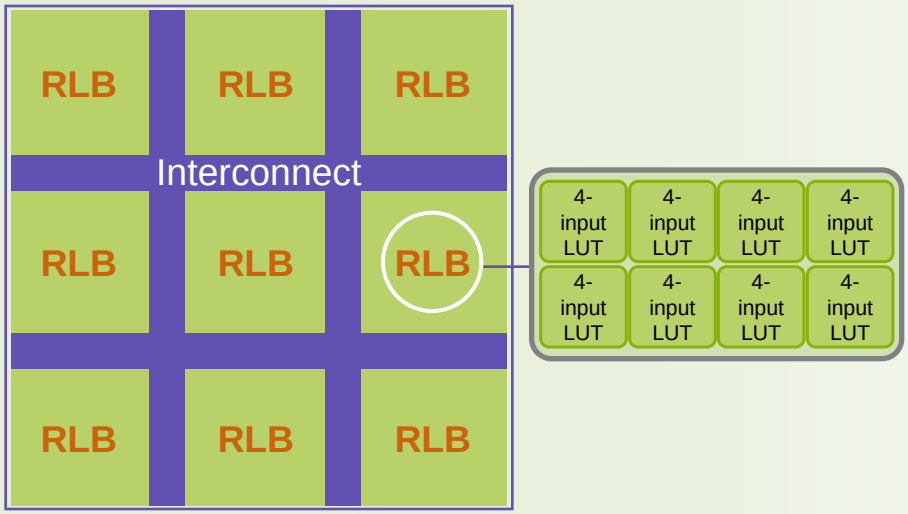
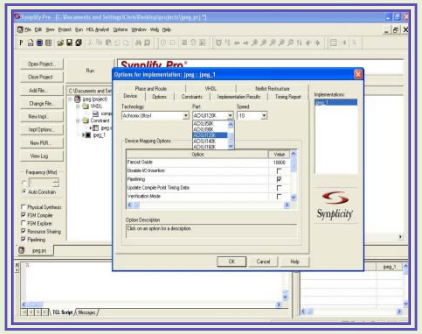
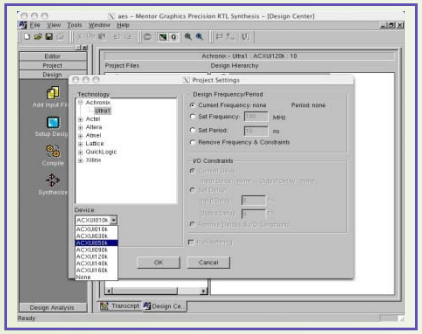
Familiar Silicon



- Traditional 4-input LUT architecture
  - With GHz performance
- SRAM-based reprogrammable FPGA
  - Uses BAE's Radiation Hardened SRAM cell

Familiar Tools





- Synplify-Pro and Mentor Precision Synthesis Flows
- Full compatibility with existing third party simulation, debug, and verification tools

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Trading off Speed for Power Dissipation: V^2f

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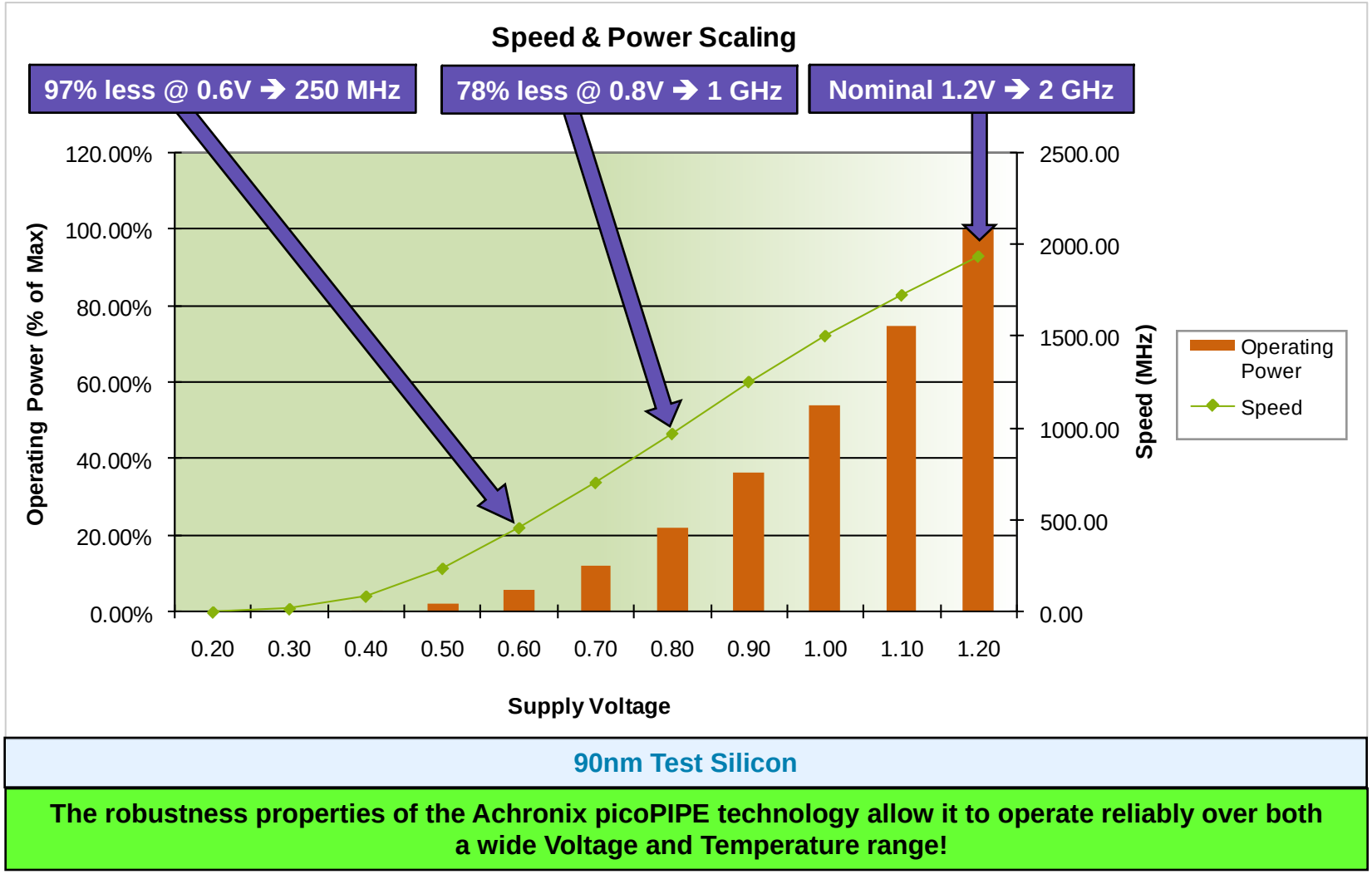

90nm Test Silicon

The robustness properties of the Achronix picoPIPE technology allow it to operate reliably over both a wide Voltage and Temperature range!

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Achronix Patented SEE Mitigation Methodology: Redundancy Voting Circuits (RVC)

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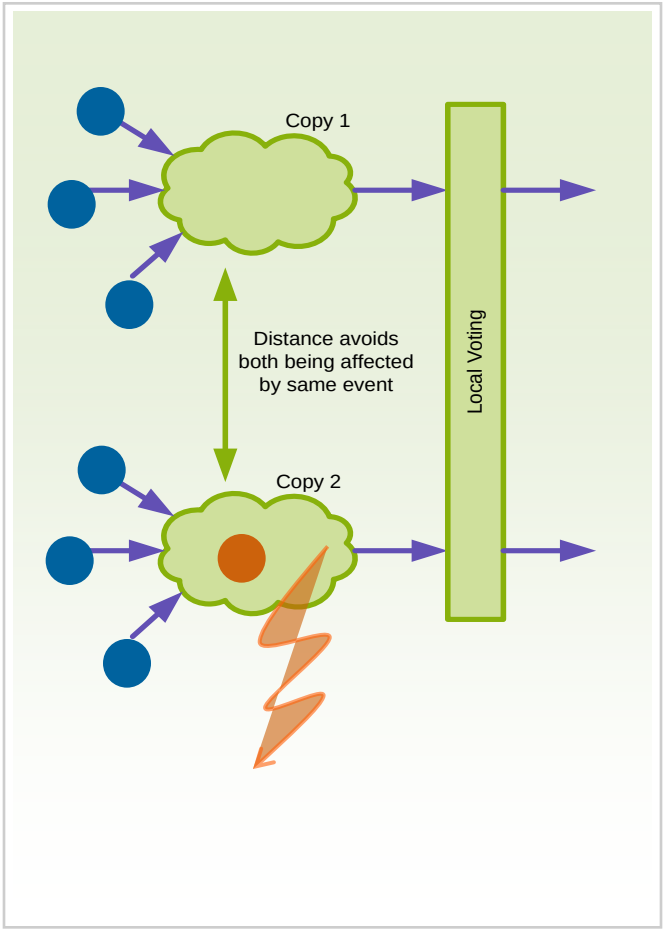
- Redundancy Voting Circuits (RVC)
  - Two copies of all circuits are implemented
  - Copies are non-adjacent to avoid the risk of a single upset affecting both
  - Every stage (combinatorial and state) has local voting mechanism

- Local voting waits until both copies agree
  - no SEE, values will agree at the voter, tokens propagate
  - When SEE occurs values won't agree at voter, local voter blocks token propagation
  - After event energy dissipates the upset circuit value is resolved to the correct value and tokens propagate



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RVC Proof of Concept Test Chip

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- Radiation Hardened By Design (RHBD) circuit techniques portable to any foundry to enable **extremely** low SEU and SET rates (< 10^{-11} upsets/bit day)
  - Circuit technique proven thru SEE testing at 150 nm applicable to any process node

Proof of Concept Vehicle	150 nm BAE Systems test chips BAE SYSTEMS
Where	Cyclotron Institute Texas A&M University
Who	NEPP NASA Electronic Parts and Packaging Program Technology for Future NASA Missions
Result	No observed SET or SEU events in SEE testing up to a LET threshold of 55 MeV-cm²/mg

Rad-Hard FPGA Test Chip & Patterns

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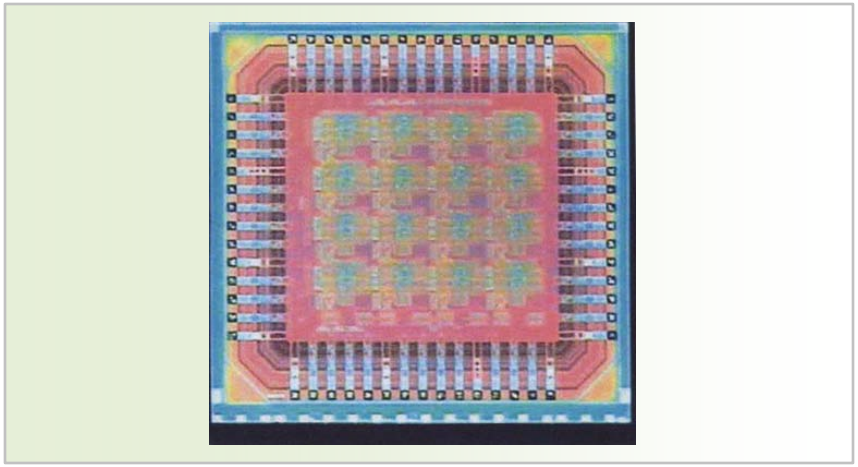
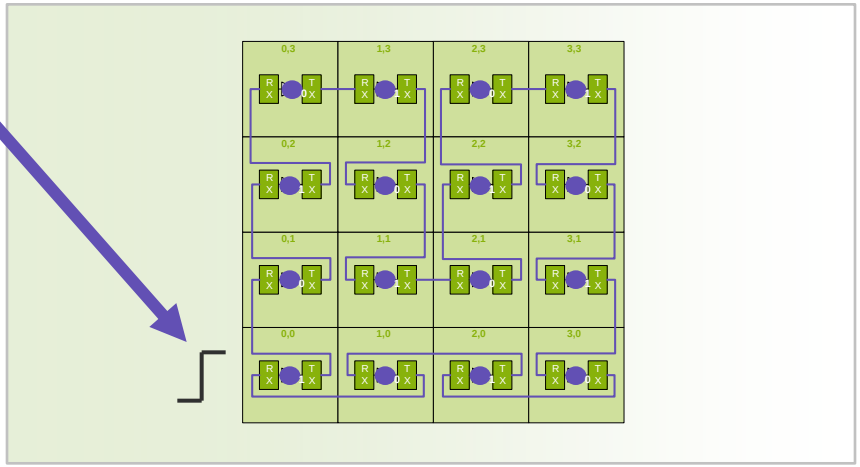
- Defined goal of initial radiation test was to prove that tokens continue to propagate in the event of heavy ion impact
- Test Chip contained a 4x4 array of FPGA Tiles implemented with RVC picoPIPE elements
- One dedicated tile had an 8 bit counter (implemented in RVC) on output acknowledge to observe the functioning of the various FPGA configurations at a reasonable frequency with standard I/O
- Five different FPGA patterns utilized during testing





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Summary: Heavy Ion SEE Test of BAE-Achronix Rad-Hard FPGA Test Chip

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- Testing completed by NASA at Texas A&M University Cyclotron Single Event Effects Test Facility (SEETF)
  - **Test Date:** August 14th, 2007
  - **Sample size:** Three devices tested including one control not exposed to the radiation source
  - **Flux:** 1 x10^3 to 1 x10^4 particles/cm^2/s
  - **Fluence:** 5x10^6 particles/cm^2
  - **Test Angles:** Normal, 45 degree
- SEL Analysis
  - No SEL observed through tests with temperatures up to 74 °C and LET of 55 MeV*cm^2/mg
- SEE Data and Analysis
  - No SEFI observed for all tests run
  - Tokens continued to propagate throughout testing

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BAE RHFPGA Process Technology

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RHFPGA Technology (RH15F) Features

Key Features

Features:	RH15
Isolation	STI
Thin Oxide / DGO Devices	26 Å / 70 Å
Vdd Options	1.5 V / 1.8 V / 3.3 V
Metal Levels	7
Capacitors	Yes
Resistors	Yes
C4 / Wirebond	Y/Y

Radiation Hardness Assurance Levels

Environment	
Total Dose (rad(Si))	1M
SEU (errors/bit-day)	1E-11
SEL (MeV-cm2/mg)	120
Neutron Fluence (n/cm2)	1E13
Prompt Dose Upset (rad(Si)/s)	1E9
Prompt Dose Survival (rad(Si)/s)	1E12

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RH15F Process Maturity - Memory

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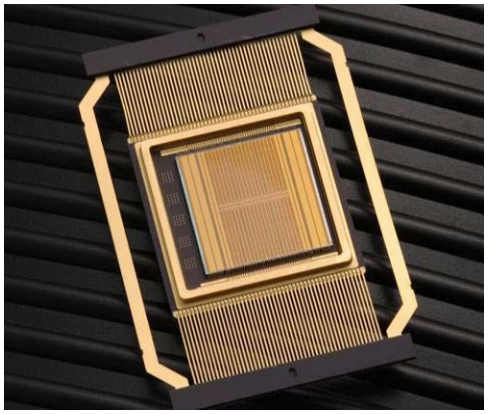
16M SRAM – Next-Generation Strategic RH SRAM



		Total ILCs	1,063,783,005
Transistors	113,070,511	CA	298,967,451
HVT NFETS	74,422,289	CT	226,146,395
HVT PFETS	38,645,756	V1	212,067,749
DGO NFETS	1,630	V2	242,233,858
DGO PFETS	836	V3	82,209,612
R2 Resistors	36,410,528	V4	1,011,258
Q2 Capacitors	18,205,264	V5	506,746
		V6	639,936

Access Time	15-20 ns
Process Technology	0.15 µm CMOS
Die Size	16 mm by 16 mm
Power Supply	1.5 V + / - 10% core 2.5 or 3.3 V + / - 10% I/O
Power Dissipation	10 mW/MHz at 1.5V (per die) 100 mW standby
Temperature Range	-55°C to +125°C
Packaging	23.2 mm by 26.2 mm by 6.0 mm 100 pin Flat Pack (5-high stack)
Radiation Hardness	Total Ionizing Dose > 1Mrad(Si) Prompt Dose > 1E9 rad(Si)/sec SEU < 1E-12 errors / bit-day (W.C. 90% GEO) Latchup: Immune
ESD	TBD
Screening level	Prototype and Flight flows
Organization	2Mx8 die – single chip package 2Mx32 4-high package 2Mx40 5-high package 512Kx32 die – single chip package

Configuration Memory Cell for RHFPGA uses the 16M SRAM Cell

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16M SRAM Heavy Ion Test Results
Memory Cell Upset

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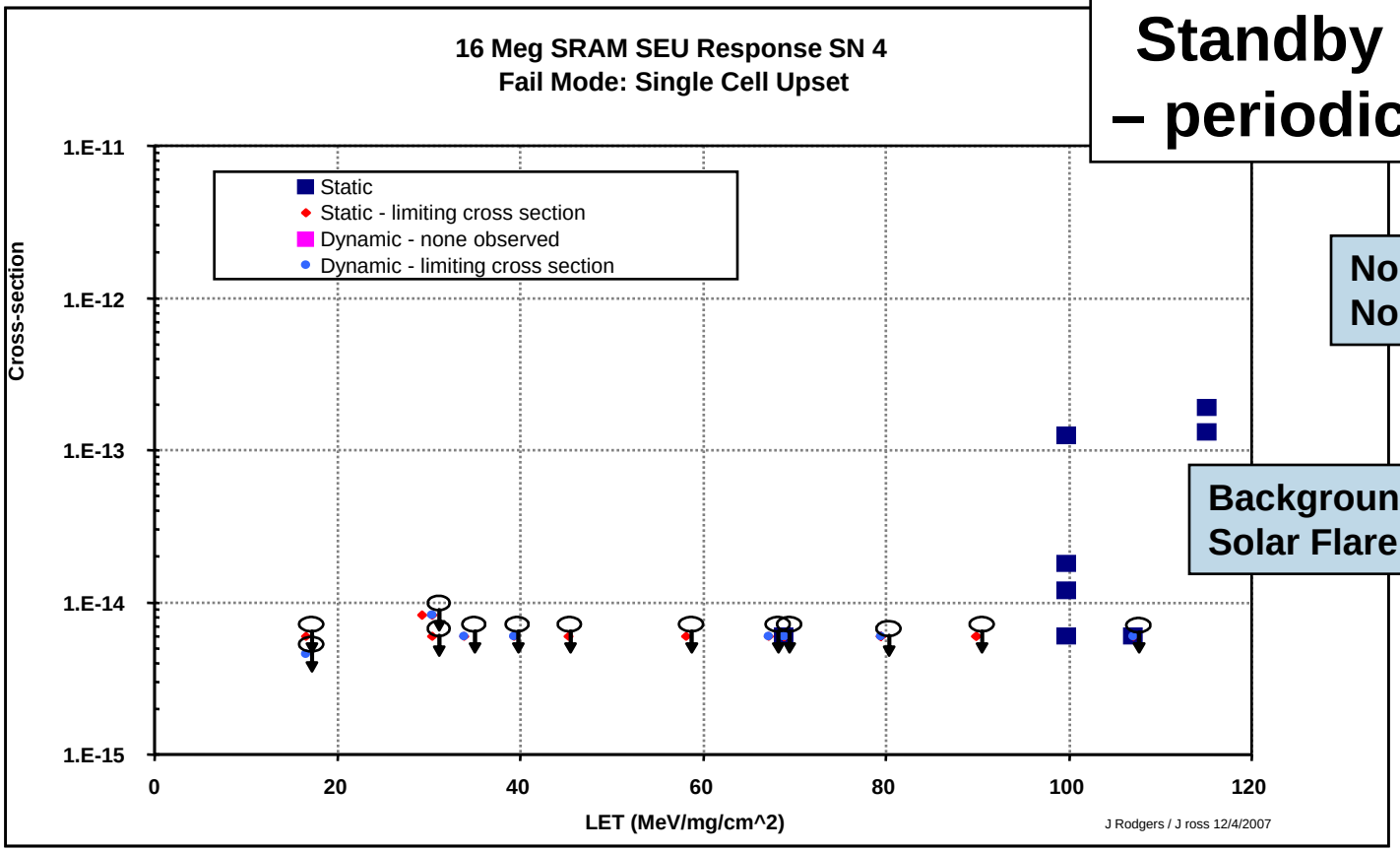

Standby mode – periodic reads

No Proton Upsets
No Latchup

Background 6e-16 u/b-d;
Solar Flare 4e-13 u/b-d

SEU for Memory Cell Exceeds RHFPGA SEU Targets

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RH15F Qualification Vehicle (16MSRAM)

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Parameter	Requirement	Goal	Achieved	Outlook
Operating Speed - worst case 125C and post radiation	≤ 20 ns	≤ 15 ns	≤ 15 ns	G
Operating Temperature Range Full Performance Functionality	0 to 80C -55C to 125C	-55C to 125C Same	-55C to 125C	G
Standby Current - worst case 125C and post radiation	≤ 60 mA	≤ 40 mA	≤ 40 mA	G
SEU (upsets/bit-day)	< 1E-10	< 1E-11	<< 1E-12	G
Total Ionizing Dose - Gamma	≥ 0.5 Mrad	≥ 1Mrad	≥ 1Mrad	G
Prompt Dose Upset (rad/sec)	≥ 1E9	≥ 1E9	Planned on 5-high stacks	G
Survivability (rad/sec)	1E12	1E12		G

Characterization complete
Qualification in progress, Prototypes Samples Available

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RHFPGA Package Definition

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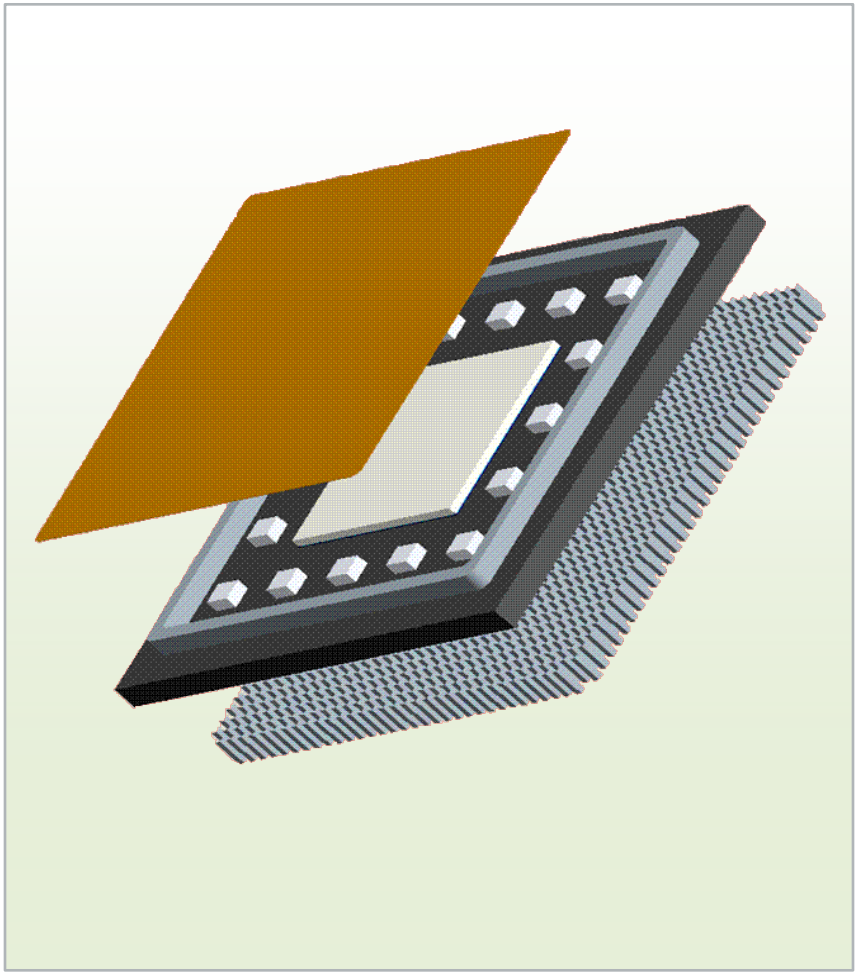
- Substrate– ceramic 32 mm x 32 mm
- 32 mm x 32 mm Column Grid Array
  - 1.27 mm pitch
  - 624 Total I/O
- Capacitors
  - Sizing suggests 16 Low Inductance Flip Chip Capacitor Sites
  - Can be used to support several different voltages
- Hermetic Seam Weld Sealing



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RHFPGA Preliminary Engineering Estimate of Part Resources

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	Radrunner Family (150 nm)		
	Device Name	**RDR500**	**RDR1000**
Device Resources	LUT	4,320	8,640
	Number of 18 Kbit Block RAM	5	10
	Block RAM (Kbit)	90	180
	Number of PLL	4	4
	SpaceWire Interfaces	4	7
	User Programmable I/O	336	384
Package	CCGA624 (32 mm x 32 mm)		384
	CQ340	286	

Design under optimization to maximize RHFPGA Resources

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SUMMARY

BAE SYSTEMS

- **Program Fulfills Critical Need for Reconfigurable RH FPGAs for Strategic Applications**
- **Excellent Partnership between BAE Systems and Achronix Ongoing**
- **Initial Achronix Commercial Chip First Pass Success**
- **Test Chip Functionality Demonstrated, Radiation Testing Successful**
- **Design Activities Continuing with No Technical Concerns**
- **Plans In Place for Further Device Enhancements**

Program Outlook Overall Positive for Initial POC Device 2Q09

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